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10/500,762	07/06/2004	Heinz Van Der Broeck	DE 020013	7172

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EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,762	VAN DER BROECK ET AL.	
	Examiner	Art Unit	
	Donna V. Lui	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *July 6, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Inventorship

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

3. The disclosure is objected to because of the following informalities: The specification must contain the appropriate headings such as the following:

a. Cross-References to Related Applications

b. Background of the Invention

i. Field of Invention

ii. Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98

c. Brief Summary of the Invention

d. Brief Description of the Drawings

e. Detailed Description of the Invention

Appropriate correction is required.

Claim Objections

4. **Claim 1** is objected to because of the following informalities:

Applicant makes reference to the auxiliary charging current and the auxiliary charging voltage as the same element. Please redefine or use separate notations such as having U1 to define the auxiliary charging current and V1 to define the auxiliary charging voltage. In the specification applicant refers to U1 as the auxiliary charging current and voltage, and thus makes determination unclear to the examiner. For the purpose of examining on merits, examiner interprets U1 as an auxiliary charging voltage.

Appropriate correction is required.

5. **Claims 3 and 24** are objected to because of the following informalities: Applicant refers to an inductor as (LA) in claim 3 and in claim 12 applicant refers to a coil as (LA). A similar situation occurs in claim 24 where applicant refers to a coil as (LB) and in claim 16 applicant refers to an inductor as (LB). Although an inductor and a coil are essentially the same thing, proper notation and consistency throughout the claim language is required. Appropriate correction is required.

6. **Claims 4, 8, 10-12, 17, 20, 21, and 25-26** are objected to because of the following informalities:

The limitations "the capacitor", "the coil", "the transistor", are referring to several different elements. Examiner would like to suggest applicant to distinguish between the elements by referring to them for example as a first capacitor, a second capacitor, a third capacitor and so on. Appropriate correction is required.

7. **Claim 19** is objected to because of the following informalities: The claim states a second diode and a second coil. The preceding independent claim does not state a first diode nor a first coil. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 1 and 29** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "... the DC converter ..." lacks antecedent basis, which makes the claim indefinite.

9. **Claim 3** recites the limitation "the boost converter" beginning at the end of line 1. There is insufficient antecedent basis for this limitation in the claim.

10. **Claim 4** recites the limitation "the three connections" in line 2. There is insufficient antecedent basis for this limitation in the claim since there exists other cases for the number of connection such as having more than three connections.

11. **Claim 16** recites the limitation "the buck convert" beginning at the end of line 1. There is insufficient antecedent basis for this limitation in the claim.

12. **Claim 17** recites the limitation "the three connections" in line 2. There is insufficient antecedent basis for this limitation in the claim since there exists other cases for the number of connection such as having more than three connections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 1-23 and 25-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai (Patent No.: 6,011,355) in view of Yao et al. (Patent No.: 5,844,373).

With respect to **Claim 1**, note the above 35. U.S.C. 112 2nd rejection. Nagai discloses a circuit arrangement for an AC voltage supply of a plasma display panel *(column 8, lines 6-8; note that the seventh embodiment builds upon previous embodiments)*, the arrangement comprising at least a transistor bridge *(See figure 6, where the transistor bridge is comprised of elements 26, 28, 38, and 39)*, an input voltage *(Vcc)*, a capacitor of the plasma cell *(See figure 19, Cp)* and a charging current circuit *(See figure 6, elements 22a and 23a)*. Nagai does not mention the charging current circuit being supplied with an auxiliary charging current, characterized in that the DC voltage converter is connected in parallel to the auxiliary charging voltage.

Yao teaches a charging current circuit *(See figure 6)* being supplied with an auxiliary charging current *(current flowing across C3)*, characterized in that the DC voltage converter *(3b ~ DC voltage converter; Note, that Va is a direct current voltage; column 4, line 66-67 and column 5 lines 24-26)* is connected in parallel to the auxiliary charging voltage *(Vw ~ charging voltage; Note that the parallel connection is at the point common to elements T1, D1, and C4)*. Yao modifies the circuit arrangement of Nagai by connecting the voltages Vw and Va respectfully to the source electrode of element 22a and 22b of Nagai, resulting in a circuit arrangement having an auxiliary charging current characterized in that the DC voltage converter connected in parallel to the auxiliary charging voltage.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a charging current circuit being supplied with an auxiliary charging current characterized in that the DC voltage converter is connected in parallel to the auxiliary charging voltage, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating a steady and smooth direct current voltage *(Yao: column 5, lines 25-26)*.

With respect to **Claim 29**, Claim 29 differs from claim 1 only in that Claim 29 is a plasma display panel comprising a circuit arrangement of claim 1 and Claim 1 is a circuit arrangement for a plasma display panel. Claim 29 and Claim 1 are essentially equivalent claims differing in that claim 1 recites the limitation "... the charging current circuit ..." and claim 29 recites the limitation "... the charging circuit ...". Claim 29 is broader than claim 1, thus claim 29 is analyzed as previously discussed with respect to claim 1.

With respect to **Claim 14**, Nagai discloses a circuit arrangement for the AC voltage supply of a plasma display panel *(column 8, lines 6-8; note that the seventh embodiment builds upon previous embodiments)*, the arrangement comprising at least a transistor bridge *(See figure 6, where the transistor bridge is comprised of elements 26, 28, 38, and 39)*, an input voltage *(Vcc)*, a capacitor of the plasma cell *(See figure 19, Cp)* and a discharging circuit *(See figure 6, elements 22b and 23b)*. Nagai does not teach the discharging circuit applying an auxiliary discharging voltage, characterized in that in addition a DC voltage converter is connected in parallel to the auxiliary discharging voltage.

Yao teaches an auxiliary discharging voltage *(See figure 6, voltage across C4)*, characterized in that in addition a DC voltage converter *(3b ~ DC voltage converter; Note, that Va is a direct current voltage; column 4, line 66-67 and column 5 lines 24-26)* is connected in parallel to the auxiliary discharging voltage *(voltage across C4 ~ discharging voltage; Note that the parallel connection is at the point common to elements T1, D1, and C4)*. Yao modifies the circuit arrangement of Nagai by connecting the voltages Vw and Va respectfully to the source electrode of element 22a and 22b of Nagai, resulting in a circuit arrangement having an auxiliary discharging current characterized in that the DC voltage converter connected in parallel to the auxiliary discharging voltage.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary discharging voltage characterized in that in addition a DC voltage converter is connected in parallel to the auxiliary discharging voltage, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating a steady and smooth direct current voltage *(Yao: column 5, lines 25-26)*. The circuit arrangement of Nagai is modified by

connecting in parallel the charging current circuit of Yao by connecting the voltage Vw and Va respectfully to the source electrode of element 22a and 22b of Nagai.

With respect to **Claim 2**, Nagai does not teach the charging current circuit is characterized in that the DC voltage converter is a boost converter.

Yao teaches a charging current circuit is characterized in that the DC voltage converter is a boost converter *(See figure 6, element 2b is a voltage booster; column 5, lines 27-34).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a charging current circuit characterized in that the DC voltage converter is a boost converter, as taught by Yao, to the circuit arrangement of Nagai for the purpose of having a stabilized voltage that is amplified to a high voltage *(Yao: column 5, lines 39-41, and column 4, lines 66-67).*

With respect to **Claim 4**, Nagai does not teach a DC converter is characterized in that the three connections of a boost converter are connected to the positive side of the capacitor, to ground and to the positive side of the capacitor.

Yao teaches a DC converter is characterized in that the connections of a boost converter are connected to the positive side of a first capacitor *(See figure 6, C4)*, to ground *(2b is connected to ground through elements T3, T4, and C3)* and to the positive side of a second capacitor *(C3)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a DC converter characterized in that the connections of a boost

converter are connected to the positive side of a first capacitor, to ground and to the positive side of a second capacitor, as taught by Yao, to the circuit arrangement of Nagai for the purpose of achieving the function of sequentially increasing the voltage Va *(Yao: Column 5, lines 39-41).*

With respect to **Claim 5**, Nagai does not the auxiliary charging voltage has a value exceeding half the value of the input voltage.

Yao teaches the auxiliary charging voltage *(See figure 6, Vw = 150 V ~ auxiliary charging voltage)* has a value exceeding half the value of the input voltage *(Vs = 180 V ~ input voltage).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have an auxiliary charging voltage value exceeding half the value of the input voltage, as taught by Yao, to the charging current circuit of Nagai so as to generate an entire-surface discharge voltage that results from adding the boosted stabilized voltage Vw to the stabilized voltage Va such that a switching regulator is unnecessary *(Yao: column 3, lines 23-29, column 4, lines 66-67, and column 5, lines 39-41)* and to provide a small-sized and economical power unit *(Yao: column 2, lines 45-47).*

With respect to **Claim 13**, claim 13 differs from claim 5 only in that claim 5 recites the limitation "... a value exceeding half the value ..." and claim 13 recites the limitation "...more than 50% of the value..." The two limitations are equivalents, thus claim 13 is analyzed as previously discussed with respect to claim 5.

With respect to **Claim 6**, Nagai teaches the charging current circuit to comprise at least a series combination of an auxiliary transistor *(See figure 6, 22a)*, a first diode *(23a)* and a first coil *(LX)*.

With respect to **Claim 7**, Nagai does not teach the charging current circuit is characterized in that the auxiliary charging voltage is applied to an auxiliary capacitor.

Yao teaches the auxiliary charging voltage *(See figure 6, Vw)* is applied to an auxiliary capacitor *(C3)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a an auxiliary charging voltage applied to an auxiliary capacitor, as taught by Yao, to the charging current circuit of Nagai for the purpose of obtaining the voltage Vw through the charging of capacitors C1, C2, and C3 *(Yao: column 5, lines 28-35 and lines 64-67)*.

With respect to **Claim 8**, Nagai does not teach the capacitance of the auxiliary capacitor is much larger than the capacitor of the plasma cell.

Yao teaches the capacitance *(See figure 6, Note that the auxiliary capacitor is a combination of C1, C2, and C3)* of the auxiliary capacitor is much larger than the capacitor *(See figure 4, 1a ~ plasma panel; the capacitor of the plasma cell is representative a one pixel)* of the plasma cell. The voltage across the capacitors C1, C2, and C3 is greater than the input voltage and the combination of the capacitors and must be larger than the capacitance of a plasma cell

since the voltage Vd *(Vd ~ Vw +Va; column 3, lines 23-29)* is for generating the entire-surface discharge voltage for the display.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a capacitance of the auxiliary capacitor to be much larger than the capacitor of the plasma cell, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating an entire-surface discharge voltage without the use of a switching regulator *(Yao: column 3, lines 23-29)* and providing a small-sized and economical power unit *(Yao: column 2, lines 45-47)*.

With respect to **Claim 9**, Nagai does not teach the auxiliary charging voltage is generated from an auxiliary discharging voltage by a DC converter.

Yao teaches an auxiliary charging voltage *(See figure 6, Vw)* is generated from an auxiliary discharging voltage *(Va)* by a DC converter *(the voltage Va is direct current, column 5, lines 25-27 and lines 32-35)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary charging voltage generated from an auxiliary discharging voltage by a DC converter, as taught by Yao to the circuit arrangement of Nagai so as to generate a constant auxiliary charging voltage since the auxiliary discharging voltage is stabilized and used to generate the auxiliary charging voltage *(Yao: column 4 lines 66-67 and column 5, lines 31-35)*.

With respect to **Claim 28**, Nagai teaches a common input voltage *(See figure 6, Vcc)* used for a plurality of independent bridge circuits *(26, 28, 38 and 39 form a bridge circuit)* but does not teach auxiliary voltages. Yao teaches auxiliary voltages *(See figure 6, Va and Vw ~ auxiliary voltages)* and the associated DC voltage converters *(3b)*. The circuit arrangement *(figure 6)* of Nagai is modified by Yao to meet the limitation of having auxiliary voltages and the associated DC voltage converters used for a plurality of independent bridge circuits, which utilize a common input voltage, by connecting the voltages Vw and Va of Yao to the source electrodes 22a and 22b respectively of Nagai.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the auxiliary voltages of Yao to the circuit arrangement of Nagai so as to output a stabilized voltage for charging *(Yao: column 4, lines 66-67)*.

With respect to **Claim 15**, Nagai does not teach a DC voltage converter is a buck converter.

Yao teaches a DC voltage converter is a buck converter *(See figure 6, the buck converter is comprised of elements To, D3 and L; column 5, lines 19-27)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a DC voltage converter that is a buck converter, as taught by Yao to the circuit arrangement of Nagai for the purpose of outputting a stabilized voltage Va *(Yao: column 4, lines 66-67)*.

With respect to **Claim 16**, Nagai does not teach a buck converter comprising a transistor, a diode and an inductor.

Yao teaches a buck converter comprising a transistor *(See figure 6, To)*, a diode *(D3)* and an inductor *(L)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a buck converter comprising a transistor, a diode, and an inductor, as taught by Yao to the circuit arrangement of Nagai for the purpose of outputting a stabilized voltage Va *(Yao: column 4, lines 66-67)*.

With respect to **Claim 17**, Nagai does not teach a buck converter where there are three connections connected to the positive side of the input voltage, to ground and to the positive side of the capacitor.

Yao teaches a buck converter *(See figure 6)* where there are three connections connected to the positive side of the input voltage *(the source of the transistor To)*, to ground *(anode of Diode D3)* and to the positive side of a capacitor *(C4)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a buck converter where there are three connections connected to the positive side of the input voltage, to ground and to the positive side of a capacitor, as taught by Yao to the circuit arrangement of Nagai so as to produce a steady and smooth direct current voltage *(Yao: column 5, lines 25-27)*.

With respect to **Claim 18**, Nagai does not teach an auxiliary discharging voltage has a value that falls short of half the value of the input voltage.

Yao teaches an auxiliary discharging voltage *(See figure 6, Va = 50 V)* has a value that falls short of half the value of the input voltage *(Vs = 180 V)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary discharging voltage having a value that falls short of half the value of the input voltage, as taught by Yao to the circuit arrangement of Nagai so as to provide a small-sized and economical power unit *(Yao: column 2, lines 45-47)* since the discharging voltage is used for generating pulses to the scanning electrodes *(Yao: column 4, lines 11-15)* and for generation of a boosted voltage *(Yao: boosted voltage ~ Vw, column 5, lines 32-35)* that is later used for generating an entire-surface discharge for the display *(Yao: Vd ~ entire-surface discharge voltage; column 3, lines 25-29)*.

With respect to **Claim 27**, Claim 27 differs from claim 18 only in that claim 18 recites the limitation "... has a value that falls short of half ..." and claim 27 recites the limitation "... is less than 50% of ..." The two limitations are equivalents, thus claim 27 is analyzed as previously discussed with respect to claim 18.

With respect to **Claim 19**, Nagai teaches the discharging circuit comprises at least a series combination of an auxiliary transistor *(See figure 6, 22b)*, a diode *(23b)* and a coil *(LX)*.

With respect to **Claim 20**, Nagai does not teach the auxiliary discharging voltage is applied to an auxiliary discharging capacitor.

Yao teaches an auxiliary discharging voltage *(See figure 6, Va)* is applied to an auxiliary discharging capacitor *(C4)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary discharging voltage applied to an auxiliary discharging capacitor, as taught by Yao to the circuit arrangement of Nagai so as to output a steady and smooth direct-current voltage through an auxiliary discharging capacitor *(Yao: column 5, lines 24-26)*.

With respect to **Claim 21**, Nagai does not teach the capacitance of the auxiliary discharging capacitor by far exceeds the capacitance of the plasma cell.

Yao teaches the capacitance *(See figure 6, Note that the auxiliary discharging capacitor is equivalent to C4)* of the auxiliary discharging capacitor by far exceeds the capacitance of the plasma cell *(See figure 4, 1a ~ plasma panel; the capacitor of the plasma cell is representative a one pixel)*. The auxiliary discharging capacitor stores the voltage for supplying pulses to the scanning electrodes; therefore the auxiliary capacitor must by far exceed that of a plasma cell since the stored voltage is for the entire display *(column 4, lines 13-15)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a capacitance value of the auxiliary discharging capacitor to by far exceed the capacitance of a plasma cell, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating pulses to all the scanning electrodes *(Yao: column 4, lines 13-15)* and

providing a small-sized and economical power unit *(Yao: column 2, lines 45-47)*.

With respect to **Claim 22**, Nagai does not teach the auxiliary discharging voltage is generated from the discharge of the capacitor and stabilized by a DC voltage converter.

Yao teaches an auxiliary discharging voltage *(See figure 6, Va)* is generated from the discharge of the capacitor *(C4)* and stabilized by a DC voltage converter *(column 4, lines 66-67; column 5, lines 24-27)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary discharging voltage generated from the discharge of the capacitor and stabilized by a DC voltage converter, as taught by Yao to the circuit arrangement of Nagai so as to use the stabilized voltage in generating a boosted voltage for a charging circuit *(Yao: column 5, lines 32-35)*.

With respect to **Claim 23**, Nagai does not teach a DC converter. Yao teaches a DC converter. The DC converter of Yao is constructed in such a way that the PWM-control IC *(Yao: figure 6, 30)* regulates the power supply voltage Va despite various variations in load *(column 5, lines 6-15)*. Referring back to the modification of the circuit arrangement of Nagai by Yao as discussed in claim 14, if loss is caused by commutation then the PWM-control IC will lengthen the "ON" period of the transistor *(To)* to compensate for the losses. Thus, Yao teaches a DC voltage converter when incorporated into the circuit arrangement of Nagai compensates for the losses caused by the commutation and takes the necessary power from the input voltage.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the DC converter of Yao to the circuit arrangement of Nagai so as to output a steady and smooth direct-current voltage *(Yao: column 5, lines 24-27)*.

With respect to **Claim 24**, Nagai does not teach the transistor via its drain has a first common connection point with the positive side of the input voltage and via its source has a common connection point with the coil and the anode of the diode.

Yao teaches a transistor *(figure 6, To)* via its source has a common connection point with the input voltage *(Vs)* and via its drain has a common connection point with the coil *(L)* and the anode of the diode *(D3)*. Please note that the source and drain are identical electrodes, thus the direction of current should not matter and the source and drain of the transistor of Yao are interchangeable.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a transistor have one electrode other than the gate electrode connected to the input voltage and the other electrode other than the gate electrode connected to the coil such that the anode of the diode is connected at the same point as the coil and electrode of a transistor, as taught by Yao to the circuit arrangement of Nagai, so as to generate a steady and smooth direct-current voltage *(column 5, lines 24-27)*.

With respect to **Claim 25**, due to the broadness of the claim there exists two alternative connections that reads on the claim limitations. The first alternative is taught solely by Nagai and

the teaching is as follows, Nagai teaches a coil *(See figure 6, LX)* connected to a transistor *(22b)* of the discharging circuit.

The second alternative is by way of the modified circuit as explained previously in the analyzing of claim 14 where the coil *(Yao: Figure 6, L)* is connected to the transistor *(Nagai: figure 6, 22b)* of the discharging circuit at the voltage Va *(Note that the elements 21 and 22b of Nagai are connected in parallel to the voltage booster 2b of Yao)*. It would haven been obvious for a person of ordinary skill in the art at the time the invention was made to modify the circuit of Nagai by connecting a coil to a transistor of the discharging circuit, as taught by Yao so as to output a steady and smooth direct-current voltage *(Yao: column 5, lines 19-27)*.

With respect to **Claim 26**, Nagao teaches a coil *(See figure 6, LX)* connected to at least a transistor *(T11)* of a charging circuit *(The connection is made by way of the diode 23a)*.

14. **Claims 3 and 10-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai and Yao as applied to claim 1 above, and further in view of Breunig et al. (Pub. No.: 2001/0023488).

With respect to **Claim 3**, Neither Nagai nor Yao teach the boost converter comprising a transistor, a diode, and an inductor.

Breunig teaches a boost converter *(See figure 2b)* comprising a transistor *(62)*, a diode *(66)*, and an inductor *(64)*. The circuit arrangement of Nagai, modified by Yao is further modified by Breunig by replacing the voltage booster *(figure 6, 2b)* of Yao with the boost

subsystem *(figure 2b, 6)* of Breunig. The input to the inductor *(Breunig: 64)* is connected to the source electrode of the transistor 22b of Nagai, the common connection point of the inductor, transistor and diode *(Breunig: 64, 62, and 66)* is connected to the direct current voltage *(Yao: Va)* and the connection point of the diode and capacitor *(Breung: 66 and 68)* is connected to the source electrode of the transistor 22a of Nagai.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a boost converter comprising a transistor, diode, and an inductor, as taught by Breunig to the circuit arrangement of Nagai as modified by Yao so as to supply voltage in the event that the input voltage supply produces an insufficient supply level *(Breunig: page 1, [0017], lines 7-11).*

With respect to **Claim 10**, Neither Nagai nor Yao teach the transistor via its source has a first connection point shared with the capacitance of the auxiliary voltage and with the ground terminal of the input voltage and via its drain has a connection point shared with the coil and the anode of the diode.

Breunig teaches a transistor *(figure 2b, 62)* via its source has a first connection point *(GND)* shared with the capacitance *(68)* of the auxiliary voltage and with the ground terminal of the input voltage *(20, the voltage supply is grounded)* and via its drain has a connection point shared with the coil *(64)* and the anode of the diode *(66)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a transistor via its source, has a first connection point shared with the capacitance of the auxiliary voltage and with the ground terminal of the input voltage, and via its

drain has a connection point shared with the coil and the anode of the diode, as taught by Breunig to the circuit arrangement of Nagai as modified by Yao so as to supply voltage in the event that the input voltage supply produces an insufficient supply level *(Breunig: page 1, [0017], lines 7-11).*

With respect to **Claim 11**, Nagai does not teach the diode with its cathode has a connection point shared with the transistor of the charging oscillator circuit and the positive side of the capacitor.

Note the modification of the circuit arrangement of Nagai by Yao as previously discussed with respect to claim 1. Yao teaches the diode *(Yao: figure 6, D1)* with its cathode has a connection point shared with the transistor *(Nagai: figure 6, 22a)* of the charging oscillator circuit and the positive side of the capacitor *(Yao: C3).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a diode with its cathode having a connection point shared with the transistor of the charging oscillator circuit and the positive side of the capacitor, as taught by Yao to the circuit arrangement of Nagai, so as to output a stabilized voltage *(column 4, lines 66-67; column 5, lines 32-35)* that is amplified and stored in the capacitor until needed for the charging oscillator circuit. Note that since the diode limits the direction of current flow the configuration allows for the charging of the capacitor C3.

With respect to **Claim 12**, Nagai teaches a coil *(figure 6, LX)* with its other end is

connected at least to the transistor *(22b)* of a discharging oscillator circuit.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huang et al. (Patent No.: 6,657,604 B2) is cited to teach an energy recover circuit for a plasma display panel using two separate inductors for charging and discharging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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